Amendments to the Drawings:

The attached sheet of drawings includes a change to FIG. 5 to add the reference number 70, which is mentioned in the specification but not shown in the figure.

Attachment: Replacement sheet 5
Annotated sheet 5 showing the change.

REMARKS

In paragraph 2 of the Office action, claims 1, 3-13, and 31-37 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1–13 and 31-41 of copending Application No. 10/689,449. Because this is a provisional obviousness-type double patenting rejection, the double patenting rejection will be addressed at such time as allowable subject matter is indicated in the instant application.

In paragraph 3 of the Office action, claims 1, 3-13, and 31-37 stand rejected under 35 U.S.C. § 101 as being direct to non-statutory subject matter. More specifically, the examiner has taken the position that the claims perform a mathematical function and do not disclose "a practical application with a concrete, useful, and tangible result, as they are pre-emptive in any application [sic]." In response, the two remaining independent claims, claims 1 and 31, have been further amended. Support for the amendments can be found in FIGs. 5 and 6 and the corresponding descriptions thereof beginning at paragraphs [0068] and [0091], respectively, of the published application.

The examiner explains on page 4 of the Office action that the claims merely disclose "elements/steps of performing mathematical function." That is not the case. Claim 1 recites:

> determining a local extrema for each of said processing elements;
>
> **serially outputting, on each clock cycle, said local extrema from each of said processing elements to a neighboring processing element until every processing element in a first dimension has received all local extrema along said first dimension;**
>
> determining within each of said processing elements a first dimensional extrema for said first dimension of said n-dimensional array, wherein said dimensional extrema is determined **concurrently with the receipt of said local extrema from said processing elements in said first dimension;**
>
> **serially outputting, on each clock cycle, said first dimensional extrema from each of said processing elements to a neighboring processing element until every processing element in a next dimension has received all first dimensional extrema along said next dimension;**
>
> determining within each of said processing elements a next dimensional extrema for a next dimension of said n-dimensional array, wherein said next dimensional extrema is determined **concurrently with the receipt of said first dimensional extrema;**
>
> **repeating said serially outputting on each clock cycle and concurrently determining** within each of said processing elements a next dimensional extrema for each of said n-

dimensions, wherein each of said next dimensional extrema is determined from a dimensional extrema from a previously selected dimension, until the global extrema is determined; and

saving said global extrema. (emphases added.)

As seen from claim 1, steps are provided to direct the movement and storage of data, and not simply the performance of mathematical functions. The highlighted language is significant because it enables the process of optimizing the operation of an n-dimensional array of processing elements. Applicant is not attempting to patent a mathematical function, but rather is attempting to patent a particular process of optimizing the operation of an n-dimensional array of processing elements. The claims, if granted, would not preempt all methods of calculating a global extrema, only the particular optimized method set forth in the claims. One of the benefits of the claimed invention is that through the combination of serially outputting data and concurrently calculating a new extrema, the global extrema can be efficiently calculated. For example, consider a 4x4x4 array of processing elements. In such an array, there are 64 local extrema. If one processing element is selected to compare its value to the values in all the other processing elements, and assuming that one comparison could be performed per clock cycle, then it would take 64 clock cycles to determine the global extrema. With the invention of claim 1, again assuming that one comparison could be performed per clock cycle, it would take 4 clock cycles to determine the extrema for the rows in the X direction, 4 clock cycles to determine the extrema for the rows in the Y direction, and 4 clock cycles to determine the extrema for the columns in the Z direction, for a total of 12 clock cycles, which represents a substantial improvement over 64 clock cycles. Note that in the process of claim 1, all of the 64 processing elements determine the global extrema, compared to the first example, in which only one processing element determines the global extrema.

Further, simply because the final result is a number does not mean that the claim is not directed to a useful, concrete, and tangible result. Optimizing the operation of an n-dimensional array of processing elements is certainly a useful exercise. The claimed optimization process is reproducible and thus concrete. The result is tangible because it enables the n-dimensional array of processing elements to operate in an efficient manner, which is a real world result.

In view of the examiner's comments, the examiner appears to believe that, for a claimed invention to achieve a "tangible result," the tangible result *must be recited as one of the elements of the claim.* That is evident by implication from the examiner's comments which note that the final result of the claimed invention is merely a number (i.e., the examiner is only looking at the claim elements and not at what the claimed invention as a whole achieves). Such a test is improper and contrary to legal precedent. The Interim Guidelines state, "[T]o be eligible for patent protection the claimed invention *as a*

whole must accomplish a practical application. That is, *it must produce* a 'useful, concrete and tangible result.'" (Interim Guidelines of 22 November 2005, first paragraph, citing *State Street Bank & Trust Co. v. Signature Financial Group, Inc.*, 149 F.3d 1368 at 1373-74 (Fed. Cir. 1998), emphasis added.) The Interim Guidelines also indicate that "[T]he focus is . . . on whether the *final result achieved* by the claimed invention is 'useful, tangible, and concrete'" (MPEP 2106 (IV)(C)(2), emphasis added). The examiner appears to have understood the words "accomplish," "produce," and "achieved" from the Interim Guidelines to mean that the claim must *recite* a tangible result as one of the elements of the claims and appears to have ignored the directive that the *claimed invention as a whole* be considered. That approach is simply incorrect.

Legal precedent makes clear that the examiner is applying an improper analysis. For example, in *In re Alappat*, 33 F.3d 1526 (Fed. Cir. 1994), the Federal Circuit reversed a decision by the Board of Patent Appeals and Interferences ("the Board") and held that Alappat's claimed invention to a rasterizer for converting vector list data representing sample magnitudes of an input waveform into anti-aliased pixel illumination intensity data to be displayed on a display means was indeed statutory under 35 U.S.C. § 101. Even though the claim at issue (claim 15) was directed to a machine, the Board argued that the claimed subject matter fell within a judicial exception as being directed to elements that merely carried out a mathematical algorithm. (*Id.* at 1542.) The Federal Circuit rejected that contention, noting that claim 15 was directed to a combination of elements for performing a combination of calculations "to transform, i.e., rastorize, digitized waveforms (data) into anti-aliased, pixel illumination data *to produce a smooth waveform.*" (*Id.* at 1544, emphasis added.) Importantly, the claim at issue *did not recite the result of "a smooth waveform,"* yet the court understood that the claimed invention as a whole produced that result in light of the description of the invention being claimed. Indeed, the Federal Circuit in *AT&T Corp. v. Excel Communications, Inc.*, 172 F.3d 1352 (Fed. Cir. 1999) explicitly commented on this aspect of *Alappat* in stating, "In *Alappat*, we held that more than an abstract idea was claimed because the claimed invention as a whole was directed toward forming a specific machine *that produced the useful, concrete, and tangible result of a smooth waveform display.*" (*Id.* at. 1357.) Again, *the claim did not recite the result of producing or displaying "a smooth waveform."* Thus, the examiner's failure to look beyond the explicit claim language for what the claimed invention as a whole achieves and the examiner's apparent requirement in the present instance that the claims themselves should recite a tangible result as one of the elements is contrary to legal precedent.

Should the examiner think that *Alappat* is distinguishable from the present matter simply because the claims at issue in *Alappat* were apparatus claims whereas certain of the present claims at issue are

method claims, it is respectfully pointed out that the Federal Circuit has already spoken to the contrary. For example, in *AT&T*, the Federal Circuit stated:

> Whether stated implicitly or explicitly, *we consider the scope of § 101 to be the same regardless of the form - machine or process - in which a particular claim is drafted.* See, e.g., *In re Alappat*, 33 F.3d at 1581, 31 USPQ2d at 1589 (Rader, J., concurring) ("Judge Rich, with whom I fully concur, reads Alappat's application as claiming a machine. In fact, *whether the invention is a process or a machine is irrelevant.* The language of the Patent Act itself, as well as Supreme Court rulings, clarifies that Alappat's invention fits comfortably within 35 U.S.C. § 101 whether viewed as a process or a machine."); State Street, 149 F.3d at 1372, 47 USPQ2d at 1600 ("[F]or the purposes of a § 101 analysis, *it is of little relevance whether claim 1 is directed to a 'machine' or a 'process,'....*"). Furthermore, the Supreme Court's decisions in *Diehr*, *Benson*, and *Flook*, all of which involved method (i.e., process) claims, have provided and supported the principles which we apply to both machine-- and process-type claims. Thus, *we are comfortable in applying our reasoning in Alappat and State Street to the method claims at issue in this case.* (172 F.3d at 1357-58, emphasis added.)

Accordingly, the insights from the Federal Circuit's analysis in *Alappat* are indeed relevant to the matter at hand.

As further evidence that the claims currently presented are directed to a statutory process, the examiner's attention is respectfully directed to the following patents, which the examiner did not comment upon in the last Office action. Although the issuance of patents in other cases is not binding on the examiner, the issuance of these patents indicates that the current claims fall within the bounds of allowable subject matter.

U.S. Patent No. 5,710,732 is entitled Calculating the Average of Four Integer Numbers Rounded Away From Zero in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an average of four unsigned operands, such that the average is an integer rounded away from zero, comprising:
>
> appending two zero's to a left end of each of the operands to provide extended operands;
>
> summing the extended operands to provide an intermediate result;
>
> removing a lowest significant bit and a second lowest significant bit from the intermediate result to provide a shortened intermediate result;
>
> incrementing the shortened intermediate result to provide the average when the removed second lowest significant bit is a one; and
>
> providing the shortened intermediate result as the average when the removed second lowest significant bit is a zero.

U.S. Patent No. 5,751,617 is entitled Calculating the Average of Two Integer Numbers Rounded Away From Zero in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an average of two unsigned operands such that the average is an integer rounded away from zero in a single instruction cycle, comprising:
>
> logically right-shifting each of the operands by one bit position, wherein bits in a lowest significant bit position of the operands become shifted-out bits;
>
> summing the right-shifted operands to obtain a result; and
>
> incrementing the result when any of the shifted-out bits is a one.

U.S. Patent No. 5,835,389 is entitled Calculating the Absolute Difference of Two Integer Numbers in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an absolute difference of first and second unsigned integer operands, such that the absolute difference is an unsigned integer, comprising:
>
> bit-complementing the second operand;
>
> summing the first and bit-complemented second operands to obtain an intermediate result;
>
> incrementing the intermediate result to obtain an incremented intermediate result;
>
> bit-complementing the intermediate result to obtain a bit-complemented intermediate result;
>
> determining whether the intermediate result overflows provided the first and bit-complemented second operands and the intermediate result are considered unsigned numbers;
>
> selecting the incremented intermediate result to obtain the unsigned absolute difference when the overflow occurs; and
>
> selecting the bit-complemented intermediate result to obtain the unsigned absolute difference when the overflow does not occur.

U.S. Patent No. 5,917,739 is entitled Calculating the Average of Four Integer Numbers Rounded Towards Zero in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an average of four signed operands, such that the average is an integer rounded towards zero in a single instruction cycle, comprising:
>
> appending two bits to a left end of each of the operands to provide extended operands, wherein for each operand the two appended bits are zero's when the operand is a positive number, and one's when the operand is a negative number,

summing the extended operands to provide an intermediate result;

removing a lowest significant bit and a second lowest significant bit from the intermediate result to provide a shortened intermediate result;

incrementing the shortened intermediate result to provide the average when the intermediate result has a negative value and either of the removed bits is a one; and

providing the shortened intermediate result as the average (i) when the intermediate result has a positive value, and (ii) when the intermediate result has a negative value and both of the removed bits are zero's.

U.S. Patent No. 6,007,232 is entitled Calculating the Average of Two Integer Numbers Rounded Towards Zero in a Single Instruction Cycle. Claim 1 reads:

1. A method of operating a circuit to obtain an average of two unsigned operands such that the average is an integer rounded towards zero in a single instruction cycle, comprising:

logically right-shifting each of the operands by one bit position, wherein bits in a lowest significant bit position of the operands become shifted-out bits;

summing the right-shifted operands to obtain a result; and

incrementing the result when both of the shifted-out bits are one's.

Claim 31 is an apparatus claim directed to an n-dimensional array of processing elements and therefore also falls within the statutory definition of patentable subject matter. See, for example, U.S. Patent No. 7,031,996 entitled Calculating Square Root of Binary Numbers with Fixed-Point Microprocessor. Claim 1 provides:

1. A square root calculator comprising:

a binary searching module operable to accept a number, perform a binary search operation, and return an integer portion of the square root of the number;

a fraction calculating module operable to calculate a fractional portion of the square root;

and a summing module operable to sum the integer portion and the fractional portion to obtain the square root.

In view of the foregoing, it is believed that the 35 U.S.C. § 101 rejection has been overcome and should now be withdrawn.

Applicant has made a diligent effort to place the instant application in condition for allowance. If the examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the examiner is respectfully requested to contact applicant's attorney at the telephone number listed below so that additional changes to the claims may be discussed.

Respectfully submitted,

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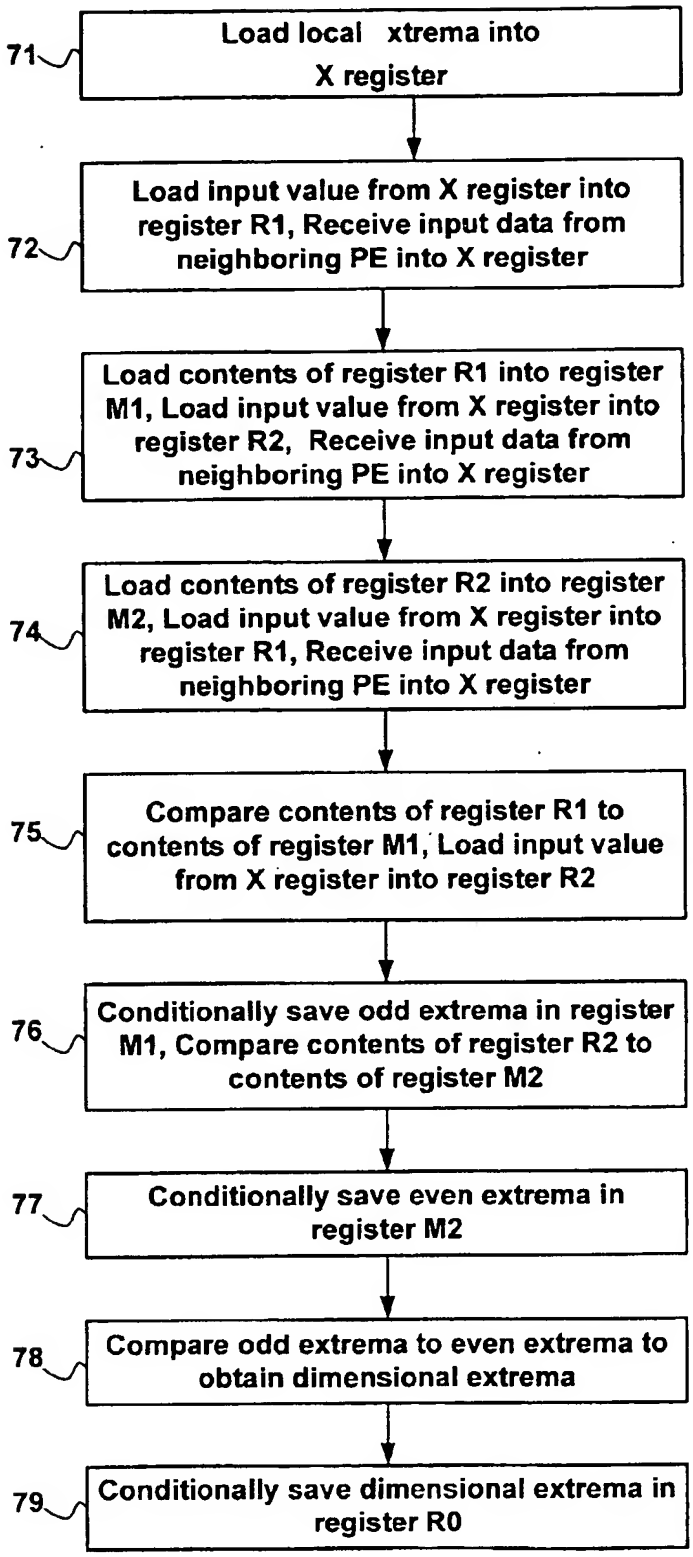
71
Load local xtrema into X register
70
72
Load input value from X register into register R1, Receive input data from neighboring PE into X register
73
Load contents of register R1 into register M1, Load input value from X register into register R2, Receive input data from neighboring PE into X register
74
Load contents of register R2 into register M2, Load input value from X register into register R1, Receive input data from neighboring PE into X register
75
Compare contents of register R1 to contents of register M1, Load input value from X register into register R2
76
Conditionally save odd extrema in register M1, Compare contents of register R2 to contents of register M2
77
Conditionally save even extrema in register M2
78
Compare odd extrema to even extrema to obtain dimensional extrema
79
Conditionally save dimensional extrema in register R0

FIG 5